IN THE SPECIFICATION

Please replace the paragraph at page 6, lines 8-12, with the following rewritten paragraph:

By using a Capacitor On Plug (COP) type structure, the area size is reduced in half compared to the offset type. However, the area of the block selecting transistor is increased. In addition, the connection between the sixth impurity-diffusion region 132 and the seventh impurity diffusion region 138 with the second metal wiring 145 may cause the area of the block selecting transistor to be determined by the density of the second ~~meal~~ metal wiring 145.

Please replace the paragraph at page 24, line 30 – page 25, line 3, with the following rewritten paragraph:

Also, a third metal plug 274 is connected to the ninth impurity-diffused region 273, a fourth metal layer 275 is connected to the third metal plug 274, and a fourth lower electrode 276 is formed over the third gate 252. Also, a fourth ferroelectric layer 277 is formed on the fourth lower electrode 276, a second dummy upper electrode 278 is formed on the fourth ferroelectric layer 277, and a first layer word line 255 is formed over the second ~~dumpy~~ dummy upper electrode 278.